Course Outline – Computer Architecture and Organization

Part A – Introduction

1.	**Course No. / Course Code**	**:** CSE 303
2.	**Course Title**	**:** Computer Architecture and Organization
3.	**Course Type**	**:** Core course
4.	**Level/Term and Section**	**:** 5th Semester (3rd Year/1st Semester)
5.	**Academic Session**	**:** Spring 2025
6.	**Course Instructor**	**:** Shaila Rahman, Assistant Professor; Shammi Akhtar, Assistant Professor
7.	**Prerequisite (If any)**	**:** CSE 209
8.	**Credit Value**	**:** 3.0
9.	**Contact Hours**	**:** 3.0
10.	**Total Marks**	**:** 100

11. Course Objectives and Course Summary:

The objectives of this course are to:

1. **Explain** the layers of computer organization.
2. **Explain** terms related to computer organization.
3. **Introduce** with clock cycle, instruction cycle, performance, instruction format, addressing mode and instruction throughput of single-cycle, multi-cycle, and pipelined implementations of a simple instruction set and pipeline hazard.
4. **Provide** the knowledge of computer hardware, memory hierarchy, cache configurations, identification, placement, replacement Strategy and Show how cache design parameters affect cache hit rate.

12. Course Learning Outcomes: at the end of the Course, the Student will be able to –

CLO 1	Explain the theoretical concepts and functional layers of computer organization, and demonstrate understanding of how these layers interact within a computer system.

CLO 2	Analyze clock cycles, instruction cycles, performance metrics, instruction formats, addressing modes, and instruction throughput for single-cycle, multi-cycle, and pipelined processor implementations.
CLO 3	Design and evaluate memory hierarchy and cache systems, including cache mapping, placement, and replacement strategies, and assess how cache parameters influence cache hit rate and overall system performance.

13. Mapping / Alignment of CLOs with Program Learning Outcomes (PLO) (Optional):

CLO No.	Corresponding PLOs (Appendix-1)	Bloom's taxonomy domain/level (Appendix-2)	Delivery methods and activities	Assessment Tools
CLO1	1	1/Understand	Lecture, multimedia, Books	Mid and Final Exam
CLO2	2	1/Analyze	Lecture, multimedia, Books	Quiz(1,2,3), Assignment, Mid and Final Exam
CLO3	3	1/Apply	Lecture, multimedia, Books	Final Exam

Part B – Content of the Course

14. Course Content:

Introduction: Computer Architecture and Organization. Instruction set architecture: Overview of MIPS, basic instruction, high level to MIPS conversion of instruction, MIPS control and data path design. Computer arithmetic and number system: Binary review; floating point number representation; basic addition and multiplication algorithm and hardware. Advanced computer arithmetic: Booth multiplication scheme, recoding process, best and worst multiplier, average gain. Computer system performance and performance matrices: Execution time, clock rate, processor speed, CPI-clock per instruction, mathematical problems. Memory and

cache hierarchy: Primary memory, secondary memory, memory hierarchy, virtual memory, caching scheme: direct addressed caching, other policies, Control design: Processor control Unit design and data path analysis, Pipelining: Pipelined data path and control, super scalar and dynamic pipelining. I/O organization: Introduction, bus control, I/O systems, programmed IO, DMA and interrupts, I/O processors, multiprocessor system: UMA, NUMA etc.

15. Alignment of topics of the courses with CLOs:

SL. No	Topics / Content	Course Learning Outcome (CLO)
1	Explain the theoretical concepts and functional layers of computer organization, and demonstrate understanding of how these layers interact within a computer system.	CLO1
2	Analyze clock cycles, instruction cycles, performance metrics, instruction formats, addressing modes, and instruction throughput for single-cycle, multi-cycle, and pipelined processor implementations.	CLO2
3	Design and evaluate memory hierarchy and cache systems, including cache mapping, placement, and replacement strategies, and assess how cache parameters influence cache hit rate and overall system performance.	CLO3

16. Class Schedule/Lesson Plan/Weekly plan:

Topics	**Specific Outcome(s)**	**Time Frame**	**Suggested Activities**	**Teaching Strategy(s)**	**Alignment with CLO**
Topic 1: Computer Abstraction and Technology Introduction to computer architecture, processor and memory technologies, performance and power wall, switching from uniprocessor to multiprocessor.	PO-a	Week 1 &2		Lecture, multimedia, Discussions	CLO1
Topic 2: Instructions: Language of the Computer Classifying instructions set	PO-b,	Week 3 to Week5		Lecture, multimedia, Web references,Discussions	CLO1,CLO2

architecture, types and size of operands, operations in the instruction set, Instruction for flow control, Instructions format, Addressing modes, MIPS Assembly Language.					
Topic 3: Arithmetic for Computers: Arithmetic Operations (Addition, Subtraction, Multiplication and Division), Floating Point Representation, Floating Point Operations (Addition and Multiplication).	PO-a, PO-b	Week 6 to Week7		Lecture, multimedia, Discussions	CLO1, CLO2,CLO3
Topic 4 : CPU Organization and Design: Datapath, pipelining, pipelined datapath and control, instruction-level parallelism)	PO-a, PO-c	Week 9 to week10		Lecture, multimedia, Problem Solving	CLO1, CLO2,CLO3
Topic 5: Cache Hierarchies Memory	PO-b, PO c	Week11 to week14		Lecture, multimedia,Problem Solving, Problem	CLO2,CLO3

hierarchies, Cache policies, Memory system, RAMs, ROMs – Speed, size and cost Performance consideration – Virtual **memory**				Solving, Group discussion	

17. Teaching-Learning Strategies:

Strategies	**Topics**
Active Learning and Discussions	Overview of Computer Architecture and Organization
Problem-Based Learning	Different Algorithms
Case-Based Learning	Architectural Design, cache memory ,pipeline strategies.

18. Assessment Techniques of each topic of the course:

SL. No	**Topics / Content**	**Assessment Techniques**
1	**Computer Abstraction and Technology** Introduction to computer architecture, processor and memory technologies, performance and power wall, switching from uniprocessor to multiprocessor.	Mid Term Exam
2	**Instructions:** Language of the Computer Classifying instructions set architecture, types and size of operands, operations in the instruction set, Instruction for flow control, Instruction's format, Addressing modes, MIPS Assembly Language.	Mid-Term Exam, Quiz-01
3	Arithmetic for Computers: Arithmetic Operations (Addition, Subtraction, Multiplication and Division), Floating Point Representation, Floating Point Operations (Addition and Multiplication)	Mid-Term Exam, Quiz-02, Final Exam

4.	CPU Organization and Design: Datapath, pipelining, pipelined datapath and control, instruction- level parallelism)	Quiz-03, Final Exam
5.	Cache Hierarchies Memory hierarchies	Quiz-04, Final Exam

Part C – Assessment and Evaluation

19. Assessment Strategy

Class Tests: Altogether 4 class tests may be taken during the semester, 2 class tests will be taken for midterm and 2 class tests will be taken for final term. 3 out of 4 class tests will be considered. Best two from Quiz-1, Quiz-2 & Quiz-3, and Quiz-4 will be considered. No makeup class tests will be taken. Students are strongly recommended not to miss any class tests.

CIE- Continuous Internal Evaluation (30 Marks)

Bloom's Category	Marks (out of 30)
Remember	
Understand	10
Apply	
Analyze	20
Evaluate	
Create	

SMEB- Semester Mid & End Exanimation (70 Marks)

Bloom's Category	**Marks (out of 70)**
Remember	
Understand	30
Apply	10
Analyze	30
Evaluate	
Create	

20. Evaluation Policy

Grades will be calculated as per the university grading structure and individual students will be evaluated based on the following criteria with respective weights.

1. Assessment 30%
2. Term Examination 50%
3. Mid-Term Examination 20%

UAP Grading Policy

Numeric Grade	Letter Grade	Grade Point
80% and above	A+	4.00
75% to less than 80%	A	3.75
70% to less than 75%	A-	3.50
65% to less than 70%	B+	3.25
60% to less than 65%	B	3.00
55% to less than 60%	B-	2.75
50% to less than 55%	C+	2.50
45% to less than 50%	C	2.25
40% to less than 45%	D	2.00
Less than 40%	F	0.00

Part D – Learning Resources

21. Text Book

1. Computer Organization and Design: The Hardware/Software Interface -David A. Patterson, John L. Hennessy (5th Edition).
2. Computer Organization & Architecture-Designing for Performance - William Stallings (6th Edition, Pearson Education).