University of Asia Pacific (UAP)

Department of Computer Science and Engineering (CSE)

BSc in CSE Program

Course Outline – Digital Logic Design

Part A – Introduction

1. **Course No. / Course Code: CSE 209**
2. **Course Title: Digital Logic Design**
3. **Course Type: Core Course**
4. **Level/Term and Section: 2nd Year 2nd Semester**
5. **Academic Session: Spring 2025**
6. **Course Instructor: Dr. Aloke Kumar Saha, Shaila Rahman**
7. **Pre-requisite (If any): Nil**
8. **Credit Value: 3**
9. **Contact Hours: 3**
10. **Total Marks: 100**
11. **Course Objectives and Course Summary:** The objectives of this course are to:

a) **Provide** knowledge and understanding on principles of digital logic operation and different types of logic gates.
b) **Introduce** the concept of different types of combinational logic, sequential circuits, registers and counters.
c) **Learn** the operation of different types of combinational logic, sequential circuits, registers and counters.
d) **Enable** the student to gain Application of different types of logic gates and flip flops.
e) **Emphasize** the Design and Implement of different types of combinational & sequential logic circuits and counters.

12. **Course Learning Outcomes: at the end of the Course, the Student will be able to –**

CLO 1	**Describe** the concept of digital logic operation and different types of logic gates.
CLO 2	**Recognize** the concept of different types of combinational logic, sequential circuits, registers and counters.
CLO 3	**Understand** the operation of different types of combinational logic, sequential circuits, registers and counters.
CLO 4	**Apply** different types of logic gates and flip flops.
CLO 5	**Design** different types of combinational & sequential logic circuits and counters.

13. Mapping / Alignment of CLOs with Program Learning Outcomes (PLO) (Optional):

CLO No.	Corresponding PLOs (Appendix-1)	Bloom's taxonomy domain/level (Appendix-2)	Delivery methods and activities	Assessment Tools
CLO1	1	1/Remember	Lecture, multimedia,	Written Examination, Assignment
CLO2	1	1/Analyze	Lecture, Group discussion	Quiz, Written Examination
CLO3	4	1/Understand	Lecture, Problem Solving, Group discussion	Quiz, Presentation, Viva, Written Examination
CLO4	5	1/Apply	Problem Solving	Quiz, Assignment, Written Examination
CLO5	5	1/Create	multimedia	Quiz, Written Examination

Part B – Content of the Course

14. Course Content:

Logic gates: Basic logic gates, compound logic gates, universal logic gates; **Boolean Algebra:** Truth tables, canonical and standard forms of functions, logic operations; **Simplification of functions:** Karnaugh map, SOP and POS methods, don't care conditions, tabulation method; **Combinational logic:** Half and full adder and subtractor, binary parallel adder, BCD adder, encoder and decoder, multiplexer and demultiplexer, Boolean function implementation using decoder and multiplexer; design and implementation of logic circuits; **Sequential logic:** Latches, flip flops, flip

flop timing consideration, flip flop excitation table; **Complex sequential logic:** Frequency division and counting, asynchronous ripple up and down counters, counters with any MOD numbers, asynchronous IC counters, propagation delay, parallel up and down counters, up/down counters, presentable counters, decoding a counter, cascading counters, shift counters; **Sequential circuits and registers:** State diagrams, state tables, state equations, flag registers, shift and parallel registers.

15. Alignment of topics of the courses with CLOs:

SL. No	Topics / Content	Course Learning Outcome (CLO)
1	Logic gates and Boolean Algebra	**CLO 1**
2	Combinational Logic Circuits, Digital Arithmetic: Operations and Circuits	**CLO 2**
3	Flip Flops and their applications, Design the various Components of Computer	**CLO 3**
4	Synchronous sequential Circuits, Asynchronous sequential Circuits	**CLO 4**
5	Counters and Registers, MSI Logic Circuits	**CLO 5**

16. Class Schedule/Lesson Plan/Weekly plan:

Topics	**Specific Outcome(s)**	**Time Frame**	**Suggested Activities**	**Teaching Strategy(s)**	**Alignment with CLO**
Logic gates and Boolean Algebra		Week 1		Lecture	CLO 1
Combinational Logic Circuits		Week 2		Lecture	CLO 2
Digital Arithmetic: Operations and Circuits		Week 3		Lecture, Problem Solving	CLO 2
Flip Flops and their applications		Week 4 & 5		Lecture, Problem Solving	CLO 3
Counters and Registers		Week 6 & 7		Lecture, Group discussion	CLO 5
MID-TERM EXAMINATION					

Counters and Registers		Week 8		Lecture, Group discussion	CLO 5
MSI Logic Circuits		Week 9 & 10		Lecture, Group discussion	CLO 5
Synchronous sequential Circuits		Week 11 & 12		Lecture, Problem Solving	CLO 4
Asynchronous sequential Circuits		Week 13 & 14		Lecture, Group discussion	CLO 4
FINAL EXAMINATION					

17. Teaching-Learning Strategies: Interactive Lectures, Google Classroom

18. Assessment Techniques of each topic of the course:

SL. No	Topics / Content	Assessment Techniques
1	Logic gates and Boolean Algebra	Written Examination, Assignment
2	Combinational Logic Circuits, Digital Arithmetic: Operations and Circuits	Quiz, Written Examination
3	Flip Flops and their applications, Design the various Components of Computer	Quiz, Presentation, Viva, Written Examination
4	Synchronous sequential Circuits, Asynchronous sequential Circuits	Quiz, Assignment, Written Examination
5	Counters and Registers, MSI Logic Circuits	Quiz, Written Examination

Part C – Assessment and Evaluation

19. Assessment Strategy

Class Tests: Altogether 4 class tests may be taken during the semester, 2 class tests will be taken for midterm and 2 class tests will be taken for final term. Out of these 4 class tests for each term best 3 class tests will be counted. No makeup class tests will be taken. Students are strongly recommended not to miss any class tests.

Assignment: The students will have to form a group of maximum 4 members. The topic or case studies will be given as assignment in groups during the class which they have to prepare at home and will submit on or before the due date. No late submission of

assignments will be accepted. Students will have to do the presentation on the given topic as assignment.

CIE- Continuous Internal Evaluation (50 Marks)

Bloom's Category Marks (out of 50)	**Tests (20)**	**Assignments (10)**
Remember		
Understand	**5**	
Apply	**10**	**5**
Analyze		**5**
Evaluate	**5**	
Create		

SMEB- Semester Mid & End Exanimation (50 Marks)

Bloom's Category	**Mid (20)**	**Final (50)**
Remember		
Understand	**10**	**15**
Apply	**3**	**20**
Analyze		
Evaluate	**7**	**15**
Create		

20. Evaluation Policy

Grades will be calculated as per the university grading structure and individual student will be evaluated based on the following criteria with respective weights.

1. Assessment 30%
2. Term Examination 50%
3. Mid-Term Examination 20%

UAP Grading Policy

Numeric Grade	Letter Grade	Grade Point
80% and above	A+	4.00
75% to less than 80%	A	3.75
70% to less than 75%	A-	3.50
65% to less than 70%	B+	3.25
60% to less than 65%	B	3.00
55% to less than 60%	B-	2.75
50% to less than 55%	C+	2.50
45% to less than 50%	C	2.25
40% to less than 45%	D	2.00
Less than 40%	F	0.00

Part D – Learning Resources

21. Text Book

Digital Systems: Principles and Applications – Ronald J. Tocci & Neal S. Widmer

Reference Books & Materials

Digital Logic and Computer Design – M. Morris Mano
Digital Fundamentals – Thomas L. Floyd