University of Asia Pacific (UAP)
Department of Computer Science and Engineering (CSE)
Course Outline

Program:	Computer Science and Engineering (CSE)
Course Title:	Digital Logic Design Lab
Course Code:	CSE 210
Semester:	Spring 2025
Level:	2nd Year 2nd Semester
Credit Hour:	1.5
Name & Designation of Teacher:	**Shammi Akhtar**, Assistant Professor. **Dr. Homeyra Akter**, Assistant Professor. **Shaila Rahman**, Assistant Professor. **Rashik Rahman,** Lecturer
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Rationale: Required course and a pre-requisite to Computer Architecture and organization (CSE 303) in the CSE program. This knowledge is very important for the Robotics and Embedded system.

Pre-requisite (if any)**: N/A**

Course Synopsis:

Boolean algebra: Verify Truth tables, canonical and standard forms of functions, logic operations.

Simplification of functions: Verify Karnaugh map, SOP and POS methods, nondegenerate terms, don't care conditions, tabulation method.

Logic gates: AND, OR, NOT and universal gates, NAND, NOR, wired-OR and wired-AND implementation.

Combinational logic: Half and full adder and subtractor, binary parallel adder, BCD adder, encoder and decoder, multiplexer and demultiplexer, Boolean function implementation using decoder and multiplexer; design and implementation of logic circuits.
Sequential logic: Latches, flip flops, flip flop excitation table.

Counters: Asynchronous and synchronous binary and BCD counters, Johnson counters and ring counters.

Synchronous sequential circuits: State diagrams, state tables, state equations, Mealy and Moore type circuits, state reduction, state assignment, incompletely specified diagrams.

Asynchronous Sequential circuits: Fundamental and pulse mode circuits, race and cycles, methods of secondary assignment.

Course Objectives: The objectives of this course are to:

1. provide knowledge and understanding on principles of digital logic operation and different types of logic gates.
2. introduce the concept of different types of combinational logic, sequential circuits, registers and counters.
3. learn the operation of different types of combinational logic, sequential circuits, registers and counters.
4. enable the student to gain Application of different types of logic gates and flip flops.
5. emphasize the Design and Implement of different types of combinational & sequential logic circuits and counters.

Course Learning Outcomes (CLO) and their mapping with Program Learning Outcomes (PLO) and Teaching-Learning Assessment methods:

CLO No.	CO Statements: Upon successful completion of the course, students should be able to:	Corresponding PLOs (Appendix-1)	Bloom's taxonomy domain/level (Appendix-2)	Delivery methods and activities	Assessment Tools	K	P	A
CLO1	Apply Boolean algebra to analyze, simplify, and verify digital logic functions using truth tables and standard techniques.	a	Apply	Multimedia, group discussion	Viva, lab work, lab report	K2	P1	
CLO2	Apply combinational logic systems, including adders, subtractors, multiplexers, and decoders, to realize specified functional requirements.	b	Apply	Multimedia, group discussion	Viva, lab work and lab report, Project	K3	P3	
CLO3	Implement and test sequential circuits, including latches, Flip-flops using logic gates and standard ICs.	b	Apply	Multimedia, group discussion	Viva, lab work and lab report	K3	P1	
CLO4	Apply standard ICs to implement and verify counters (asynchronous, synchronous, BCD, Johnson, ring) with timing analysis.	b	Analyze	Multimedia, group discussion	Viva, lab work and lab report, set-up test	K3	P3	
CLO5	Undertake a design project to integrate combinational and sequential logic components into a functional digital subsystem.	c	Create	Multimedia, group discussion	Presentation and project report	K5	P7	

CLO6	Communicate technical information effectively through project reports, presentations, and viva in the context of digital system design.	j	Apply	Group discussion	Viva,Project report, Project presentation			A1, A5

Weighting COs with Assessment methods:

Assessment Type	% weight	CLO1	CLO2	CLO3	CLO4	CLO5	CLO6
Continuous Lab Assessment	**50%**	**10**	**10**	**10**	**10**	**0**	**10**
Lab set-up test	**20%**				**20**		
Project presentation followed Viva	**30%**					**15**	**15**
Total	**100%**	**10**	**10**	**10**	**30**	**15**	**25**

Grading Policy: As per the approved grading policy of UAP (Appendix-3)

Course Content Outline and mapping with Cos

Weeks	Topics / Contents	Course Outcome	Delivery methods and activities	Reading Materials
01	Test and verify the truth table of following gates: AND gate, OR gate, NOT gate, NAND gate, NOR gate, Exclusive OR gate.	CLO1	Lecture	To be assigned during the lecture
02	a) Simplify the given logic expression and verify the truth table. b) Design a logic circuit from a given problem.	CLO1	Lecture	To be assigned during the lecture

03	a) Test and verify the Universality of NAND gate. b) Test and verify the Universality of NOR gate.	CLO1	Lecture	To be assigned during the lecture
04	a) Design 1 bit Half Adder and Full Adder b) Test and verify the 4-bit parallel Adder (IC # 7483) c) Design Subtractor using IC # 7483 d) Adder + Subtractor e) Design a 4 bit adder subtractor with full adders.	CLO2	Lecture	To be assigned during the lecture
05	Design a 4-bit ALU with 4-bit parallel adder (IC# 7483) and logic gates	CLO2	Lecture, Group discussion	To be assigned during the lecture
06	a) Implement and verify SR Latch with NAND and NOR gate.	CLO3	Lecture, Group discussion	To be assigned during the lecture
07	Project Presentation	CLO5, CLO6		
08	a) Test and verify the truth table of Clocked D flip-flop (IC#7474) b) Implement a clocked D flip-flop. c) Test and verify the truth table of Clocked JK flip-flop (IC#7476). d) Implement a clocked JK flip-flop.	CLO3	Lecture, Group discussion	To be assigned during the lecture
9	a) Design and verify MOD 8 asynchronous up counter. b) Design and verify MOD 8 asynchronous down counter. c) Design and verify MOD 8 asynchronous up/down counter. d) Design and verify MOD 10 asynchronous up counter.	CLO4	Lecture, Group discussion	To be assigned during the lecture

10	a) Design and verify MOD 8 synchronous up counter. b) Design and verify MOD 8 synchronous down counter. c) Design and verify MOD 8 synchronous up/down counter. d) Design and verify MOD 10 synchronous up counter.	CLO4	Lecture, Group discussion	To be assigned during the lecture
11	a) Design and verify 4 bit Ring counter. b) Design and verify a 4 bit johnson counter. c) Using IC#74293 (IC #7493 for proteus) design MOD 8, MOD 10, MOD 13, MOD 16, MOD 60 counter.	CLO4	Lecture, Group discussion	To be assigned during the lecture
12	a) Test and verify the 1 of 8 decoder (IC# 74LS138 & IC#74HC238). b) Test and verify the 8 input MUX (IC# 74151). c) Design and implement a 4 bit Logic unit using a MUX. AND, OR, XOR, NOT	CLO2	Lecture, Group discussion	To be assigned during the lecture
13	Project Presentation	CLO5, CLO6		
14	Lab Final + Viva	CLO4		

Required References: Digital Systems: Principles and Applications – Ronald J. Tocci & Neal S. Widmer

Recommended References: Digital Logic and Computer Design – M. Morris Mano
Digital Fundamentals – Thomas L. Floyd

Special Instructions:

Students must come to the class prepared for the course material covered in the previous class(es).
They must submit their assignments on time.
No late or partial assignments will be acceptable. There will be no make-up quizzes.

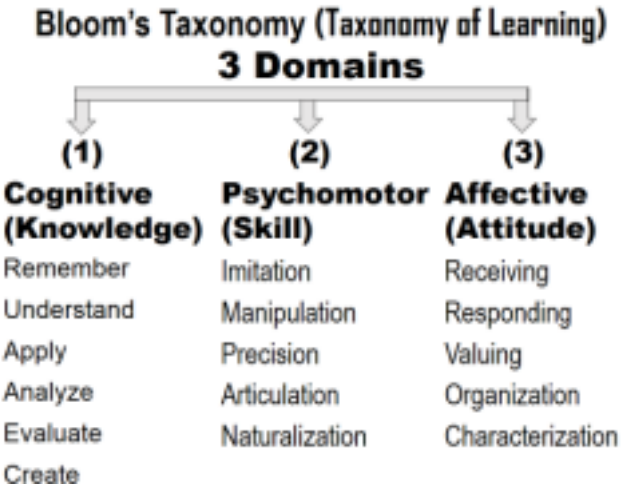
Prepared by	Checked by	Approved by
Shaila Rahman, **Shammi Akhtar,** **Dr. Homeyra Akter,** **Rashik Rahman**	Chairman, PSAC committee	Head of the Department

Appendix-1:

Washington Accord Program Outcomes (PO) for engineering programs:

No.	PO	Differentiating Characteristic
1	Engineering Knowledge	Breadth and depth of education and type of knowledge, both theoretical and practical
2	Problem Analysis	Complexity of analysis
3	Design/ development of solutions	Breadth and uniqueness of engineering problems i.e. the extent to which problems are original and to which solutions have previously been identified or codified
4	Investigation	Breadth and depth of investigation and experimentation
5	Modern Tool Usage	Level of understanding of the appropriateness of the tool
6	The Engineer and Society	Level of knowledge and responsibility
7	Environment and Sustainability	Type of solutions.
8	Ethics	Understanding and level of practice
9	Individual and Team work	Role in and diversity of team
10	Communication	Level of communication according to type of activities performed
11	Project Management and Finance	Level of management required for differing types of activity
12	Lifelong learning	Preparation for and depth of Continuing learning.

Appendix-2



Appendix-3: Grading Policy

Numeric Grade	Letter Grade	Grade Point
80% and above	A+	4.00
75% to less than 80%	A	3.75
70% to less than 75%	A-	3.50
65% to less than 70%	B+	3.25
60% to less than 65%	B	3.00
55% to less than 60%	B-	2.75
50% to less than 55%	C+	2.50
45% to less than 50%	C	2.25
40% to less than 45%	D	2.00
Less than 40%	F	0.00